

## **OPTIMIZING IC CLOCK STRUCTURES BY MINIMIZING CLOCK UNCERTAINTY**

### ABSTRACT OF THE DISCLOSURE

Clock uncertainty between a receiving cell and a  
5 launching cell of a net is estimated by back-tracing  
a first path from the receiving cell toward the clock  
source and marking each cell having a predetermined  
character along the first path. A second path from  
the launching cell toward the clock source is back-  
10 traced to a predetermined marked cell. Clock  
uncertainty is calculated based on the portion of the  
first path from the predetermined marked cell to the  
receiving cell. Clock uncertainty is calculated if a  
slack does not exceed a margin value. In one  
15 embodiment, a clock net in the form of a tree is  
optimized by forcing a first buffer to the center of  
gravity of a plurality of buffers having nets without  
timing violations to maximize a common path from the  
root to the forced buffer and minimize the non-common  
20 paths from the forced buffer to the leaves, thereby  
minimizing clock uncertainty.